memory cores laid out so that no two memory cores of the same memory bank share a common sense amplifier.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on November 15, 2002, and the references cited therewith. In response thereto, claims 57-60 are added. As a result, claims 1-60 are now pending in this application. The original claims 1-57 have not been amended. Reconsideration of the claims is respectfully solicited.

PLEASE NOTE: This response was due Saturday, February 15, 2003, which according to 37 C.F.R. §1.7, allows for the timely filing of a response on Monday, February 17, 2003. Since Monday, February 17, 2003, was a Federal Holiday in the District of Columbia (Presidents Day), the response is considered timely filed on Tuesday, February 18, 2003. Since all Federal Offices were closed on Tuesday, February 18, 2003, due to the extreme snowstorm in the Washington D.C. area, and Tuesday, February 18, 2003, is therefor considered a Federal Holiday within the District of Columbia (see attached Official Notice from the United States Patent and Trademark Office), this response is considered timely filed on Wednesday, February 19, 2003. Thus, no extension of time is necessary for this response.

IN THE DRAWINGS

The drawings were objected to under 37 C.F.R. 1.83(a) since the drawings allegedly did not show every feature of the invention specified in the claims. The feature of the memory cores from two of the different ones of the plurality banks are interleaved in a strip/row with the plurality of shared sense amplifiers as recited in claims 1-56 and their connective relationship is alleged to be missing.

As described in connection with the argument against the rejections under 35 U.S.C. § 112, second paragraph, Applicant maintains that the strip 370 and the connective relationships are already shown in Figure 3. In the interest of expediting prosecution and furthering a better understanding of the present invention, Applicant proposes the attached photocopy of Figure 3 with changes indicated in red ink. The drawing includes dashed lines identifying strip 370 in

Figure 3 to more clearly distinguish the horizontal strip which shows how the memory cores from two of the different ones of the plurality banks are interleaved in a strip/row with the plurality of shared sense amplifiers as recited in claims 1-56. No new matter has been added since reference number 370 already identifies the strip. Reconsideration and removal of the drawing objection and approval of the new drawing change is respectfully solicited.

35 U.S.C. §112 Rejection of the Claims

Claims 1-56 were rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The Office Action stated that it was not clear "how the memory cores from two of the different ones of the plurality banks are interleaved in a strip/row with the plurality of shared sense amplifiers as recited in claims 1-56."

The strips of rows and columns in Figure 3 are described in the specification of the patent application. First, with respect to Figure 1, "rows," "columns" and "strips" are defined. With regard to Figure 1, it states:

> Figure 1 shows a prior art multi-bank memory device. Memory device 100 includes memory cells arranged in rows and columns. Each column is shown as a vertical strip of memory cells, and each row is shown as a horizontal strip of memory cells. For example, strip 102 is a column that includes memory cells 120, 124, and 128, and strip 104 is a column that includes memory cells 130, 134, and 138. In memory device 100, each column corresponds to a single bank of memory cores. For example, memory cores 120, 124, and 128 of strip 102 are part of Bank 0, and memory cores 130, 134, and 136 of strip 104 are part of Bank 1. As shown in Figure 1, memory device 100 is arranged into "n" banks labeled Bank 0 through Bank (n-1). Specification, page 2, lines 6-14.

With regard to Figure 3, the same naming conventions are followed for defining horizontal and vertical strips. The specification states:

> Figure 3 shows a multi-bank memory device in accordance with the present invention. Memory device 300 includes memory cells arranged in rows and columns. Each column is shown as a vertical strip of memory cells, and each row is shown as a horizontal strip

of memory cells. For example, strip 302 is a column that includes memory cells 320, 324, and 328, and strip 370 is a row that includes memory cells 320 and 330. As shown in Figure 1, memory device 100 is arranged into "n" banks labeled Bank 0 through Bank (n-1). Specification, page 5, lines 19-25.

Thus, strip 370 as referenced and identified in the original drawing for Figure 3, already identifies a strip which is a column having the memory cores from two of the different ones of the plurality of banks interleaved in a strip with the plurality of shared sense amplifiers. Strip 370 includes core 320 from Bank 0 and core 330 from Bank 1 sharing sense amplifier 340. Thus the drawings and the specification support the claims. Applicant respectfully submits that claim 1-56 are not in violation of 35 U.S.C. § 112, first paragraph since there is adequate support and description for the invention. Reconsideration of the rejection, removal of the rejection and allowance of all claims is respectfully solicited.

35 U.S.C. §103 Rejection of the Claims

Claims 1-56 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohsawa (U.S. 5,970,016) in view of Morton (U.S. 5,159,572). Applicant respectfully traverses this rejection on several grounds described below. For the reasons stated, Applicant has deemed that the claims do not require amendment since they already distinguish over the art of record.

All Elements of the Claims are not Present in the Combination

The Ohsawa patent describes a DRAM device with memory banks capable of independent operation, such as Rambus and the like. (Ohsawa, col. 1, lines 7). This architecture is similar to the architecture shown in Applicant's patent application in conjunction with Figure 1. As a result of this architecture, the Ohsawa patent suffers from the same noise problems in Multi-bank operation as described by Applicant in conjunction with Figure 1. However, Ohsawa does not recognize the problem or provide a solution for the sense amplifier noise resulting from adjacent column decode lines being active at the same time during simultaneous multi-bank operation.

The Morton patent describes a very old DRAM architecture which uses distributed row address decode and uses interleaved word line signals in a cell array. For example, Figure 3 of

the Morton patent shows cell array 26 having rows of cells being address from both word line decode units 48 and 48' (see arrows alternating in left and right directions). This use of the term "interleaving" refers only to local word lines and has nothing to do with alternating banks of memory. Further, the Morton patent describes a traditional DRAM from approximately 13 years ago which was not capable of simultaneous access of multiple banks of memory such as the type found in the Ohsawa patent. Hence, the Morton patent fails to teach an interleaving of different ones of a plurality of banks in a strip with shared sense amplifiers. Morton also fails to describe sense amplifiers which are shared between banks of memory (there are no banks of memory in Morton). Morton and Ohsawa also fail to even identify any noise problems in sense amplifiers associated with multiple memory bank access.

Since all of the elements of the claimed invention are not found in the combination of references cited in the First Office Action, the rejection of claims 1-56 under 35 U.S.C. §103(a) must fail. Applicant respectfully requests reconsideration of the claims and allowance of all claims.

The Motivation to Combine is Nowhere Taught in the Combination

Applicant has identified a potentially serious problem associated with simultaneous multi-bank access in Rambus-type architecture. Noise from adjacent firing column decoder lines can have an adverse impact on proper sensing in sense amplifiers.

To arrive at the Applicant's claimed invention by combining the Ohwasa and Morton patents as proposed by the examiner, one of ordinary skill in the art would have had to find the elements of the claims in the references *and* show the motivation to combine the references somewhere in the referenses themselves. Applicant respectfully submits that the examiner has not provided the required explanation as to why the applied prior art itself would have provided one of ordinary skill in the art with a motivation to make this substitution and a reasonable expectation of success in doing so. *See In re Vaeck,* 947 F.2d 488, 493, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991); *In re O'Farrell,* 853 F.2d 894, 902, 7 USPQ2d 1673, 1680 (Fed. Cir. 1988).

The examiner's argument that it would have been obvious under 35 U.S.C. § 103(a) for one of ordinary skill in the art at the time the invention was made to modify Figure 1 of Ohwasa

by teaching as taught in Figure 3 of Morton "for the purpose of lower manufacturing cost and reliability" (citation to Morton, column 5, lines 64-68 and column 6, line 1-12) is not sufficient for carrying the burden of presenting a prima facia case of obviousness since the cited portion of Morton has nothing to do with the problem identified or the solution achieved. A broad conclusion that one skilled in the art would move in the technical direction of the present invention "to lower manufacturing cost" is not a motivation to combine the specific features of the two references to achieve the Applicant's claimed solution.

For this and the other reasons cited above, Applicant respectfully requests reconsideration of the claims and allowance of all claims.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612-373-6904) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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By their Representatives,

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Date Feb. 19, 2003 By Daniel J. Kluth
Daniel J. Kluth
Reg. No. 32,146

CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 19th day of February, 2003.

Amy Moriarty
Name

Amy Moriarty
Signature